



Patent Application

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANTS: Allen et al. DOCKET: YOR920030406US1 (8728-649)  
SERIAL NO: 10/733,210 GROUP ART UNIT: 2825  
FILED: December 10, 2003 EXAMINER: Dinh, Paul  
FOR: FRAMEWORK FOR HIERARCHICAL VLSI DESIGN

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Commissioner for Patents  
P.O. Box 1450  
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**RESPONSE UNDER 37 U.S.C. 1.116**

Examiner:

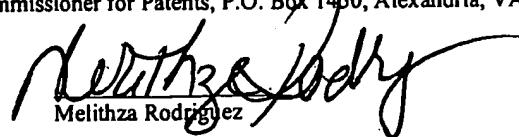
This reply is in response to the Final Office Action dated November 22, 2005. Please consider the following remarks.

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Dated: January 23, 2006



Melithza Rodriguez